



## UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
 United States Patent and Trademark Office  
 Address: COMMISSIONER FOR PATENTS  
 P.O. Box 1450  
 Alexandria, Virginia 22313-1450  
 www.uspto.gov



Bib Data Sheet

CONFIRMATION NO. 4886

<b>SERIAL NUMBER</b> 10/812,962	<b>FILING OR 371(c) DATE</b> 03/31/2004 <b>RULE</b>	<b>CLASS</b> 361	<b>GROUP ART UNIT</b> 2841	<b>ATTORNEY DOCKET NO.</b> OKI 417	
<b>APPLICANTS</b> Seiichiro Sasaki, Tokyo, JAPAN; Kouji Morita, Saitama, JAPAN; <b>** CONTINUING DATA</b> <i>None</i> <i>yes</i> <b>** FOREIGN APPLICATIONS</b> <i>yes</i> <i>yes</i> JAPAN 397724/2003 11/27/2003 <b>IF REQUIRED, FOREIGN FILING LICENSE GRANTED</b> <b>** 06/10/2004</b>					
Foreign Priority claimed <input checked="" type="checkbox"/> yes <input type="checkbox"/> no 35 USC 119 (a-d) conditions <input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after met Verified and <i>Yuri Sasaki</i> <i>10</i> <i>ys</i> Acknowledged <i>Examiner's Signature</i> <i>Initials</i>		<b>STATE OR COUNTRY</b> JAPAN	<b>SHEETS DRAWING</b> 5	<b>TOTAL CLAIMS</b> 15	<b>INDEPENDENT CLAIMS</b> 3
<b>ADDRESS</b> RABIN & BERDO, P.C. Suite 500 1101 14th Street Washington, DC20005					
<b>TITLE</b> Multilayered power supply line for semiconductor integrated circuit and layout method thereof					
<b>FILING FEE RECEIVED</b> 770	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees ( Filing ) <input type="checkbox"/> 1.17 Fees ( Processing Ext. of time ) <input type="checkbox"/> 1.18 Fees ( Issue ) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit		